ECE 5755: Digital Signal Processing Laboratory

Spring 2016

Logistics

Co-requisite:	ECE 4750/6750 or equivalent.
Instructor:	Daniel Weller Assistant Professor, ECE Office: Rice 309 Phone: (434) 924-4271 Email: <u>dweller@virginia.edu</u> [Include "ECE 5755" in the title/subject]
	Office Hours: TBD
Assistant(s):	ТВА
Lecture:	Date/time: Tuesdays, 2:00 PM – 4:45 PM Room: Thornton Hall E225
Textbook:	none required.

Course Description

The lab complements the ECE 4750/6750 Digital Signal Processing (DSP) course by providing experience designing and understanding real digital signal processing systems. This class involves a series of weekly labs (some multi-week) that connect DSP concepts learned in the class with practical experiments using LabVIEW and MATLAB software in conjunction with NI hardware. Each lab culminates in a detailed write-up. These lab reports are the major assignments in this course.

Learning Goals and Objectives

This course is aimed at $3^{rd}/4^{th}$ year undergraduates interested in understanding how to analyze and design real-world digital signal processing systems. By the end of this course, students should be able to:

- 1. Design and implement a DSP system using tools like LabVIEW and MATLAB
- 2. Analyze and describe the functionality of a real world DSP system
- 3. Work in teams to plan and execute the creation of a complex DSP system
- 4. Apply DSP system design to real world applications

Evaluation

Lab Reports (100%): Each individual is required to write up a complete report for each weekly or multiweek lab assignment. These reports must introduce the lab objectives, provide necessary background, describe in detail the methods and experimental procedures, depict and thoroughly discuss experimental results and observations, and conclude with a summary of the completed objectives. These reports also must list the contributions of each team member and answer all questions mentioned in the lab assignment. Each report will be due one week after the lab is finished, at 11:55 PM that evening, and must be submitted via Collab in PDF format. **Attendance of each lab during the scheduled time is highly recommended**; due to high use of the room, students should not rely on after-hours access to complete their assignments.

Course Policies and Grading

Cheating: This course is governed by the UVA honor code policy. If you are unfamiliar with this policy or have questions, please contact me. In particular, you are expected to do your own work and not to provide assistance to others on individual activities. Plagiarism or copying code or solutions, even with attribution, is considered cheating. Course materials should not be shared or distributed outside this class.

Attendance: Students are expected to attend all labs and read through the lab assignments in advance. If you are unable to attend a lab, it is your responsibility to notify your lab partner(s) and make alternative arrangements with your partner(s) and me. Inability to attend the lab does not excuse you from completing the lab report on time.

Late Policy: Unless prior arrangements are made with me, late assignments will lose 10% value each day after the deadline. No late assignment will be graded after a week after the deadline.

Disabilities: Students who need to make arrangements for disabilities should work with the Student Disability Access Center or other appropriate office and provide me with documentation detailing the accommodations requested. All reasonable efforts will be made to ensure these needs are met.

Grading: Grades will be assigned according to this scale: 93=A / 90=A- / 87=B+ / 83=B / 80=B- / 77=C+ / 73=C / 70=C- / 67=D+ / 63=D / 60=D- / below=F. I may adjust these thresholds downward to reflect the actual difficulty of the class, but I will not set these thresholds above what are listed here.